TRANSMITTAL OF APPEAL BRIEF	Docket No. 49581/P042US/10315832

In re Application of: Robert A. Greene

Application No.	Filing Date	Examiner	Group Art Unit
10/807,789-Conf. #4254	March 24, 2004	L. Pham	2814

Invention: SYSTEM AND METHOD FOR COUPLING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT TO THE INTEGRATED CIRCUIT'S PACKAGE PINS

TO THE COMMISSIONER OF PATENTS:

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Dated: January 16, 2007

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Docket No.: 49581/P042US/10315832
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Robert A. Greene

Application No.: 10/807,789 Confirmation No.: 4254

Filed: March 24, 2004 Art Unit: 2814

For: SYSTEM AND METHOD FOR COUPLING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT TO THE INTEGRATED CIRCUIT'S PACKAGE PINS

Examiner: L. Pham

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under 37 C.F.R. § 41.37(a), this brief is filed within two months of the Notice of Appeal filed concurrently herewith, and is in furtherance of said Notice of Appeal.

The fees required under 37 C.F.R. § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument
VIII. Claims Appendix
IX. Evidence Appendix
X. Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Microtune (Texas), L.P.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 43 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 20
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-19 and 21-44
4. Claims allowed: none
5. Claims rejected: 1-19 and 21-44

C. Claims On Appeal

The claims on appeal are claims 1-19 and 21-44.

IV. STATUS OF AMENDMENTS

A Final Office Action rejecting the claims of the present application was mailed October 20, 2006. In response, Applicant did not file an Amendment After Final Rejection, but instead files a Notice of Appeal, which this brief supports. Accordingly, the claims on appeal are those as rejected in the Final Office Action of October 20, 2006. A complete listing of the claims is provided in the Claims Appendix hereto.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the separately argued claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. It should be noted that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

According to one claimed embodiment, such as that of independent claim 1 , an integrated circuit (100) comprises internal circuitry (101, 103) and a package (102) having at least two pins (108, 109). The integrated circuit further comprises a first carrier (110) communicatively coupling said internal circuitry (103) with a first one (108) of said at least two pins, wherein said first carrier (110) carries a signal (114) of a first polarity; and a second carrier (111) communicatively coupling said internal circuitry (103) with said first one (108) of said at least two pins, wherein said second carrier (111) carries a signal (115) of a polarity opposite said first polarity. The integrated circuit further comprises a third carrier (112) communicatively coupling said internal circuitry (103) with a second one (109) of said at least two pins, wherein said third carrier (112) carries a signal 114) of said first polarity; and a fourth carrier (113) communicatively coupling said internal circuitry (103) with said second one (109) of said at least two pins, wherein said fourth carrier (113) carries a signal (115) of a polarity opposite said first polarity.

In certain embodiments, such as that of dependent claim 12, said first one (108) and said second one (109) of said at least two pins are electrically coupled together to form a common electrical node, *see e.g.,* pins 108 and 109 coupled together to form a common electrical node in FIGURE 1.

According to one claimed embodiment, such as that of independent claim 18, a method comprises coupling (e.g., block 601 of FIGURE 6) a first carrier (110) from an internal resonant frequency circuitry (103) of an integrated circuit (100) to an electrically common interface (e.g., the electrically common interface formed by pins 108 and 109 in FIGURE 1) of the integrated circuit's package (102), wherein said first carrier (110) is arranged to carry signals (114) of a first polarity. The method further comprises coupling

(e.g., block 602 of FIGURE 6) a second carrier (111) from said internal resonant frequency circuitry (103) of said integrated circuit (100) to said electrically common interface (e.g., pins 108 and 109) of the integrated circuit's package (102), wherein said second carrier (111) is arranged to carry signals (115) of a polarity opposite said first polarity. The method further comprises coupling (e.g., block 603 of FIGURE 6) a third carrier (112) from said internal resonant frequency circuitry (103) of said integrated circuit (100) to said electrically common interface (e.g., pins 108 and 109) of the integrated circuit's package (102), wherein said third carrier (112) is arranged to carry signals (114) of said first polarity.

According to one claimed embodiment, such as that of independent claim 32, a system comprises a resonant tank circuitry (103) implemented in a package (102) that provides a plurality of interface means (e.g., pins 108 and 109) that are electrically coupled together to form an electrically common interface. The system further comprises a first coupling means (e.g., bond wire 110) for communicatively coupling said resonant tank circuitry (103) to one (108) of said plurality of interface means (108,109), wherein said first coupling means (110) carries a signal (114) of a first polarity. The system further comprises a second coupling means (111) for communicatively coupling said resonant tank circuitry (103) to one (108) of said plurality of interface means (108,109), wherein said second coupling means (111) carries a signal (115) of polarity opposite said first polarity.

According to one claimed embodiment, such as that of independent claim 39, a system comprises internal circuitry (101, 103) implemented in a package (102) that provides a plurality of pins (e.g., pins 108, 109). The system further comprises a first plurality of carriers (110, 111) communicatively coupling said internal circuitry (103) to a first one (108) of said plurality of pins, wherein said first plurality of carriers (110, 111) are used as inductors for said internal circuitry (103), and wherein at least one (110) of said first plurality of carriers carries a signal (114) of a first polarity and at least one other (111) of said first plurality of carriers carries a signal (115) of polarity opposite said first polarity. The system further comprises a second plurality of carriers (112, 113) communicatively coupling said internal circuitry (103) to a neighboring pin (109) of said first one (108) of said plurality of pins, wherein said second plurality of carriers (112, 113) are used as inductors for said internal circuitry (103), and wherein at least one (112) of said second plurality of carriers carries a signal (114) of said first polarity and at least one other (113) of said second plurality

of carriers carries a signal (115) of polarity opposite said first polarity; and said first plurality of carriers (110, 111) and said second plurality of carriers (112, 113) arranged to interleave the polarities of signals (114, 115) carried thereby.

In certain embodiments, such as that of dependent claim 44, the first one pin (108) and said neighboring pin (109) are electrically coupled together to form a common electrical node, *see* the common electrical node formed by the coupling of pins 108 and 109 in FIGURE 1.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-19 and 21-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,909,034 to Soldavini et al. (hereinafter "*Soldavini*") in combination with Published U.S. Patent Application No. 2005/0116013 to Kwark et al. (hereinafter "*Kwark*") and U.S. Patent No. 5,165,590 to Cini et al. (hereinafter "*Cini*") and Published U.S. Patent Application No. 2005/0212604 t Cyr et al (hereinafter "*Cyr*").

VII. ARGUMENT

Appellant respectfully traverses the outstanding rejections of the pending claims, and requests that the Board reverse the outstanding rejections in light of the remarks contained herein. The claims do not stand or fall together. Instead, Appellant presents separate arguments for various independent and dependent claims. Each of these arguments is separately argued below and presented with separate headings and sub-heading as required by 37 C.F.R. § 41.37(c)(1)(vii).

A. Claim Rejections Under 35 U.S.C. § 103

Claims 1-19 and 21-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Soldavini* in combination with *Kwark* and *Cini* and *Cyr*. Appellant respectfully traverses these rejections below, and therefore respectfully requests that the Board overturn the rejections.

To establish a prima facie case of obviousness, three basic criteria must be met. *See* M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to

combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combination of references must teach or suggest all the claim limitations. Without conceding any other criteria, Appellant respectfully asserts that the combination of references fails to teach or suggest all the limitations of claims 1-19 and 21-44, and insufficient motivation exists for combining the references in the manner applied by the Final Office Action, as discussed further below.

Independent Claim 1 and Dependent Claims 2-11 and 13-17

Independent claim 1 recites:

> An integrated circuit comprising:
> internal circuitry;
> package having at least two pins;
> a first carrier communicatively coupling said internal circuitry with a first one of said at least two pins, wherein said first carrier carries a signal of a first polarity;
> a second carrier communicatively coupling said internal circuitry with said first one of said at least two pins, wherein said second carrier carries a signal of a polarity opposite said first polarity;
> a third carrier communicatively coupling said internal circuitry with a second one of said at least two pins, wherein said third carrier carries a signal of said first polarity; and
> a fourth carrier communicatively coupling said internal circuitry with said second one of said at least two pins, wherein said fourth carrier carries a signal of a polarity opposite said first polarity.

As discussed below, the applied references fail to teach or suggest all elements of claim 1, and insufficient motivation exists to combine the references in the manner applied by the Final Office Action. In particular, the applied references fail to teach or suggest carriers (e.g., bonding wires) coupled to a common pin and carrying signals of opposite polarity, such as the first and second carriers coupled to the first one of the at least two pins and carrying signals of opposite polarity, as recited by claim 1, and no motivation exists for modifying the references to do so, as explained further below.

The Final Office Action relies upon *Soldavini* as teaching the recited first and second carriers coupled to the first pin (citing carriers 44a and 44b coupled with pin 27 in figure 3 of *Soldavini*) and third and fourth carriers couple to the second pin (citing carriers 44a and 44b

coupled with pin 30 in figure 3 of *Soldavini*). *See* page 2 of the Final Office Action. The Final Office Action states that *Soldavini* teaches that the carriers "have polarity, but fail to teach the carriers coupled to the same pin have opposite polarity." Page 2 of the Final Office Action. The Final Office Action asserts that *Kwark* teaches that coupling of carriers having opposite polarity reduces the effective impedance, and thus concludes that it would have been obvious to have carriers or bonding wires coupling to a pin having opposite polarity in the device of *Soldavini* to achieve the benefit of reducing the effective impedance, *see* page 3 of the Final Office Action. Appellant respectfully disagrees as discussed below.

As discussed in the previous responses dated February 23, 2006 and July 26, 2006 (hereinafter "previous responses") and further below, *Soldavini* provides a device in which a common signal is carried from a node to a pin. For instance, as shown in Figure 3 of *Soldavini*, node 24 is connected to pin 29 via two parallel wires 44a and 44b (*see* col. 3, line 66 – col. 4, line 14 of *Soldavini*). The signal is carried from the node to the pin using two parallel wires in order to reduce resistivity and increase current capacity. As was explained in the previous responses, this is analogous to implementing a highway having two lanes for traffic flowing in one direction (as opposed to only one lane of traffic flowing in the direction) so as to reduce the "resistivity" along the highway in such direction. *Cini* similarly explains that where multiple bond wires are used to couple an integrated circuit to an external pin, a greater amount of current may be transmitted in one direction. *See Cini* at col. 2 lns. 9-15. Thus, *Soldavini* teaches that in order to take advantage of the teachings, the two wires coupled to a common pin must carry signals having the same polarity. Therefore, while *Soldavini* discloses coupling multiple bond wires between a node and a pin, the very object of *Soldavini* of reducing resistivity requires that the multiple wires coupled to given pin carry signals having the same polarity, rather than signals of opposite polarity as recited by claim 1.

Kwark describes configurations of bond wires for: 1) "single-ended signals" (where the signal has one component that is compared to a ground reference), and 2) differential signals ("i.e., signals of opposite polarity"). For single-ended signals, *Kwark* teaches placing one wire carrying the signal in close proximity to another wire carrying the ground reference. *See Kwark* at [0031]. For differential signals, *Kwark* teaches placing the two wires carrying

the differential signal in close proximity to each other. *See Kwark* at [0046]. However, *Kwark* does not teach or suggest that the adjacent bonding wires carrying signals of opposite polarity would be coupled to a common pin. Rather, the adjacent bonding wires carrying signals of opposite polarity in *Kwark* are coupled to different pins. More specifically, in Figure 4, *Kwark* teaches using a pair of ribbon bonds in differential signaling, where the ribbon bonds connect to microstrips 403 and contact pads 406. *See Kwark* at [0058]. Note that each ribbon bond originates from and connects to a separate contact point – there are two microstrips and two contact pads such that the two ribbon bonds originate and terminate at different points.

Accordingly, the relied upon teachings of *Soldavini* and *Kwark* fail to teach or suggest carriers (e.g., bonding wires) coupled to a common pin and carrying signals of opposite polarity, such as the recited first and second carriers coupled to the first one of the at least two pins and carrying signals of opposite polarity, as recited by claim 1. That is, *Soldavini* expressly teaches coupling a plurality of bonding wires to a common pin that carry signals having the same polarity, and must do so to achieve its desired goal of reducing resistivity. And, *Kwark* teaches placing two wires carrying differential signals (of opposite polarity) in close proximity to each other, but the two wires are coupled to separate contact points rather than to a common pin. Thus, neither reference discloses coupling carriers to a common pin for carrying signals of opposite polarity. Further, there is no motivation to combine the *Soldavini* and *Kwark* references in a manner as to modify the *Kwark* reference to couple its bonding wires that carry signals of opposite polarity to a common pin, or as to modify the *Soldavini* reference to have its bonding wires that are coupled to a common pin carry signals of opposite polarities, as discussed further herein. Indeed, as mentioned above, to so modify *Soldavini* would defeat the very object of *Soldavini* of reducing resistivity for signals traveling in a common direction.

The Final Office Action asserts that *Kwark* teaches a configuration that reduces effective impedance, *see* page 3 of the Final Office Action. The Final Office Action then asserts that it would have been obvious to one of ordinary skill in the art to combine the teachings of *Kwark* with *Soldavini* in order to achieve the benefit of reduced effective impedance. However, the Final Office Action has failed to identify any motivation to

combine. To form a proper rejection, the Examiner must identify some motivation in the references themselves or in the knowledge available to one of ordinary skill in the art. See M.P.E.P. § 2143. Here, the Final Office Action has merely identified a benefit of *Kwark*, but has not identified any motivation for applying that benefit to the teachings of *Soldavini*. Further, as noted above, no such motivation exists because modifying *Soldavini* in the manner suggested by the Examiner (i.e., to have the wires coupled to a common pin carry signals of opposite polarity) would defeat the very object of *Soldavini*, and it appears to alter the principle of operation of *Soldavini* as one is left to question how the device of *Soldavini* would work under the Examiner's proposed configuration.

In response to the above argument, the Final Office Action asserts the following on page 11 thereof:

> In response to the applicant's arguments ..., it is submitted that Kwark et al. is being relied only for the broad teaching of coupling of carriers or bonding wires having opposite polarity to reduce effective impedance.

However, Appellant notes that the applied references as a whole must be considered, including those teachings that would lead one of ordinary skill away from the proposed combination and/or modification being applied by the Examiner. So, *Kwark's* teachings cannot properly be considered in a vacuum as being solely relied upon for the teaching of coupling carriers or bonding wires having opposite polarity to reduce effective impedance, while ignoring all other teachings of *Kwark* regarding how the bonding wires are so coupled. As noted above, the configuration of coupling the bonding wires that carry opposite polarity in *Kwark* does not have the wires coupled to a common pin. As further noted above, the express teaching of *Soldavini* proposes multiple bonding wires coupled to a common pin that carry signals of the same polarity. These express teachings of the applied references that would strongly lead one of ordinary skill in the art away from the combination/modification proposed by the Examiner cannot properly be ignored in relying solely on *Kwark* "only for the broad teaching of coupling of carriers or bonding wires having opposite polarity to reduce effective impedance".

The Final Office Action further asserts on pages 11-12 thereof:

> In response to the applicant's arguments ..., it is submitted that Kwark et al. clearly teach the motivation for coupling of carriers or bonding wires having opposite polarity that is to reduce effective impedance. See [0046] of Kwark et al. Further, it is submitted that the fact that the applicants have a different reason or advantage resulting from doing what the relied prior art suggested doing is not indicative or demonstrative of unobviousness. In Re Kronig 190 USPQ 425, 428 (CCPA 1976); In Re Lintner 173 USPQ 560 (CCPA 1972). Further, it is submitted that the prior art motivation or advantage may be different that that of applicants while still supporting a conclusion of obviousness. In Re Wiseman 201 USPQ 658 (CCPA); Ex Parte Obiaya 227 USPQ 58 (Bd. of App. 1985). In this particular case, kwark et al. teach bonding wires having opposite polarities to improve connections whereas Soldavini et al. teach bonding wires to reduce resistance.

Appellant disagrees for several reasons. First, *Kwark* merely provides motivation for coupling bonding wires having opposite polarity to separate pins in order to reduce effective impedance. *Kwark* provides no teaching or suggestion of coupling bonding wires having opposite polarity to a common pin. Further, *Kwark* provides no motivation for doing so, particularly when considered in light of the express teaching of *Soldavini* in which multiple bonding wires are coupled between pins where such wires have the same polarity, for reducing resistivity along the path. Thus, while *Kwark* may suggest that multiple bonding wires carrying signals of opposite polarity can reduce impedance, *Kwark* merely suggests an arrangement in which the bonding wires are coupled to separate pins. Further, *Soldavini* provides no motivation for coupling the wires carrying separate polarity to a common pin because the express goal of *Soldavini* relies upon the multiple wires that are coupled to a common pin carrying the same polarity signals, as discussed above.

Further, as the Final Office Action asserts, the prior art motivation may be different than the motivation of the Applicant. However, the Final Office Action must still point to some valid motivation, not merely recite an advantage of one of the references. *Soldavini* and *Kwark* teach disparate techniques for designing wire bonds to address disparate problems. While it may be possible to combine the two techniques, neither *Kwark* nor *Soldavini* provides any such motivation and the Final Office Action has not identified any. By simply identifying component parts and describing the advantage for each component

part, the Final Office Action has engaged in impermissible hindsight reconstruction. *See In re Fina*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Further, certainly no motivation has been identified that would lead one of ordinary skill in the art to combine the teachings of *Kwark* and *Soldavini* in the manner proposed by the Examiner, particularly considering that such a way of combining the references would defeat the very goal and principle of operation of *Soldavini*. For instance, even if one were motivated to combine the teaching of *Kwark* with that of *Soldavini*, one would *not* construct the claimed apparatus recited by claim 1. As mentioned above, the two wires that are coupled to a common pin in *Soldavini* do not have opposite polarity, but are instead two parallel transmissions of a single-ended signal from a single node. The signal is split in parallel in *Soldavini* to reduce resistivity (e.g., make a two-lane highway with traffic flowing in the same direction) and increase current capacity. Thus, in the nomenclature of *Kwark*, *Soldavini* teaches a single-ended signal that has been split in parallel onto two bonding wires.

If one were motivated to combine the teaching of *Kwark* with that of *Soldavini* at all, one would apply the singled-ended signal teachings of *Kwark* to the configuration of *Soldavini* so as to not defeat the goal expressly taught by *Soldavini* of having the bonding wires coupled to a common pin carry signals of the same polarity (to reduce resistivity). Thus, if attempting to incorporate the teaching of *Kwark* with *Soldavini* one would be motivated, if at all, to place a bond wire (or a pair of bond wires) carrying the ground reference in close proximity to the bond wires carrying the single-ended signal in parallel where the two signal-carrying bond wires terminate at one pin and the ground bond wire(s) terminates at another pin. Such a configuration is different than the configuration of claim 1 in two respects. First, claim 1 involves transmission of signals with two polarities, not a single-ended signal and a ground signal. Second, claim 1 recites two pairs of carriers, each pair carrying signals of opposite polarity coupling to a single pin.

Further, *Cini* and *Cyr* are not relied upon for resolving the above deficiencies of *Soldavini* and *Kwark*, nor do they do so.

Further, page 12 of the Final Office Action asserts that: "In response to the applicant's arguments in part of the first full paragraph on page 12 of the amendment dated 07/26/06, it is

submitted that limitations that are argued but not recited in present claims have not considered." It is unclear as to what limitations the Examiner refers as being argued but not recited. As noted above, claim 1 expressly recites that two carriers for carrying signals of opposite polarity are coupled to a common pin. For instance, claim 1 first recites:

> a first carrier communicatively coupling said internal circuitry with a first one of said at least two pins, wherein said first carrier carries a signal of a first polarity;
> a second carrier communicatively coupling said internal circuitry with said first one of said at least two pins, wherein said second carrier carries a signal of a polarity opposite said first polarity....

Thus, the first and second carriers are communicatively coupled with the recited first one of the at least two pins, and the second carrier carries a signal of polarity opposite that carried by the first carrier. Further, claim 1 also recites:

> a third carrier communicatively coupling said internal circuitry with a second one of said at least two pins, wherein said third carrier carries a signal of said first polarity; and
> a fourth carrier communicatively coupling said internal circuitry with said second one of said at least two pins, wherein said fourth carrier carries a signal of a polarity opposite said first polarity.

Thus, the third and fourth carriers are communicatively coupled with the recited second one of the at least two pins, and the fourth carrier carries a signal of polarity opposite that carried by the third carrier. It is exactly these elements, which are recited, that Appellant has argued as not being taught or suggested by the applied references, and that insufficient motivation exists for modifying the applied references to include these elements.

In view of the above, Appellant respectfully requests that the Board overturn the rejection of claim 1.

Also, dependent claims 2-11, 13-14, and 17 depend either directly or indirectly from claim 1, thus inheriting all of the limitations of independent claim 1. These claims are believed to be allowable over the applied combination of references for at least the reasons presented above for claim 1. Therefore, Appellant respectfully requests that the Board overturn the rejection of claims 2-11 and 13-17.

Dependent Claim 12

Dependent claim 12 depends from claim 1, and thus inherits all of the limitations of claim 1 in addition to its own supplied limitations. It is respectfully submitted that dependent claim 12 is allowable at least because of its dependence from claim 1 for the reasons discussed above.

Claim 12 further recites "wherein said first one and said second one of said at least two pins are electrically coupled together to form a common electrical node." (Emphasis added). The applied combination of references further fails to teach or suggest this element of claim 12. The Final Office Action asserts on page 4 thereof that *Soldavini* teaches this element in that it teaches a first one (27) and a second one (30) of its pins being electrically coupled together via internal circuitry to form a common electrical node. Appellant respectfully disagrees. While, the separate pins of *Soldavini's* circuit may be electrically coupled together via the internal circuitry, they are not coupled to form a common electrical node. Rather, the separate pins provide separate electrical nodes with disparate inputs/outputs present thereon at any given time. Integrated circuits commonly include separate pins that are electrically coupled by internal circuitry. For instance, a first pin may be for receiving power, another pin may be for ground, another pin may be for outputting a first output signal, while still another pin may be for outputting a different output signal. Such pins, as in the case of *Soldavini*, do not provide a common electrical node, but rather each provide a disparate node on which a different input/output signal may be present at any give time.

Cini, *Cyr*, and *Kwark* are not relied upon for resolving the above deficiencies of *Soldavini*, nor do they do so.

Thus, for this further reason, the rejection of claim 12 should be overturned.

Independent Claim 18 and Dependent Claims 19 and 21-31

Independent Claim 18 recites:

> A method comprising:
> coupling a first carrier from an internal resonant frequency circuitry of an integrated circuit to an electrically common interface of the integrated circuit's package, wherein said first carrier is arranged to carry signals of a first polarity;
> coupling a second carrier from said internal resonant frequency circuitry of said integrated circuit to said electrically common interface of the integrated circuit's package, wherein said second carrier is arranged to carry signals of a polarity opposite said first polarity; and
> coupling a third carrier from said internal resonant frequency circuitry of said integrated circuit to said electrically common interface of the integrated circuit's package, wherein said third carrier is arranged to carry signals of said first polarity.

The applied combination fails to teach or suggest all elements of claim 18. As discussed above with claim 1, the combined teachings of *Soldavini* and *Kwark* fail to teach or suggest a coupling a first, second, and third carrier to an electrically common interface where the first and third carrier carry signals of a first polarity and the second carrier carries a signal of an opposite polarity. As mentioned above with claim 12, the disparate pins (e.g., pins 27 and 30) of *Soldavini* do not form an electrically common interface, but instead form disparate interfaces. That is, even through the separate pins may be electrically coupled together via internal circuitry, they are not so coupled as to form a common interface, but instead form disparate interfaces on which different input/output signals may be present at any given time.

Cini and *Cyr* are not relied upon as teaching this element, nor do they do so. As further discussed above with claim 1, one of ordinary skill in the art would not be motivated to combine the teachings of *Kwark* with *Soldavini* in the manner applied by the Final Office Action.

In view of the above, Appellant respectfully requests that the the rejection of claim 18 be overturned.

Also, dependent claims 19 and 21-31 depend either directly or indirectly from claim 18, thus inheriting all of the limitations of independent claim 18. These claims are believed to be allowable over the applied combination of references for at least the reasons presented above for claim 18. Therefore, Appellant respectfully requests that the Board overturn the rejection of claims 19 and 21-31.

Independent Claim 32 and Dependent Claims 33-38

Independent claim 32, as amended herein, recites:

> A system comprising:
> resonant tank circuitry implemented in a package that provides a plurality of interface means that are electrically coupled together to form an electrically common interface;
> first coupling means for communicatively coupling said resonant tank circuitry to one of said plurality of interface means, wherein said first coupling means carries a signal of a first polarity; and
> second coupling means for communicatively coupling said resonant tank circuitry to one of said plurality of interface means, wherein said second coupling means carries a signal of polarity opposite said first polarity.

The applied combination fails to teach or suggest all elements of claim 32. As discussed above, neither *Soldavini* nor *Kwark* teaches or suggests a plurality of interface means that are electrically coupled together to form an electrically common interface. The Final Office Action asserts, on page 4 thereof that *Soldavini*'s pins 27, 30 provide a plurality of interface means that are electrically coupled together. Appellant respectfully submits that the pins 27, 30 are not electrically coupled together so as to form an electrically common interface. Rather, the pins 27 and 30 provide disparate interfaces that output disparate signals at any given time. Further, one of ordinary skill in the art would not be motivated to combine the teachings of *Soldavini* with *Kwark* for the reasons discussed above. Additionally, neither *Cini* nor *Cyr* are relied upon for resolving the above deficiencies of *Soldavini* and *Kwark*, nor do they do so.

Thus, the rejection of claim 32 should be overturned.

Also, dependent claims 33-38 depend either directly or indirectly from claim 32, thus inheriting all of the limitations of independent claim 32. These claims are believed to be allowable over the applied combination of references for at least the reasons presented above for claim 32. Therefore, Appellant respectfully requests that the Board overturn the rejection of claims 33-38.

Independent Claim 39 and Dependent Claims 40-43

Independent claim 39 recites:

> A system comprising:
> internal circuitry implemented in a package that provides a plurality of pins;
> a first plurality of carriers communicatively coupling said internal circuitry to a first one of said plurality of pins, wherein said first plurality of carriers are used as inductors for said internal circuitry, and wherein at least one of said first plurality of carriers carries a signal of a first polarity and at least one other of said first plurality of carriers carries a signal of polarity opposite said first polarity;
> a second plurality of carriers communicatively coupling said internal circuitry to a neighboring pin of said first one of said plurality of pins, wherein said second plurality of carriers are used as inductors for said internal circuitry, and wherein at least one of said second plurality of carriers carries a signal of said first polarity and at least one other of said second plurality of carriers carries a signal of polarity opposite said first polarity; and
> said first plurality of carriers and said second plurality of carriers arranged to interleave the polarities of signals carried thereby.

The applied combination fails to teach or suggest all elements of claim 39. As discussed above with claim 1, the combined teachings of *Soldavini* and *Kwark* fail to teach or suggest a first and second plurality of carriers that are coupled to a common pin which carry signals of opposite polarity. As further discussed above with claim 1, one of ordinary skill in the art would not be motivated to combine the teachings of *Kwark* with *Soldavini* in the manner applied by the Final Office Action. Additionally, neither *Cini* nor *Cyr* are relied upon for resolving the above deficiencies of *Soldavini* and *Kwark*, nor do they do so.

Thus, the rejection of claim 39 should be overturned.

Also, dependent claims 40-43 depend either directly or indirectly from claim 39, thus inheriting all of the limitations of independent claim 39. These claims are believed to be

allowable over the applied combination of references for at least the reasons presented above for claim 39. Therefore, Appellant respectfully requests that the Board overturn the rejection of claims 40-43.

Dependent Claim 44

Dependent claim 44 depends from claim 39, and thus inherits all of the limitations of claim 39 in addition to its own supplied limitations. It is respectfully submitted that dependent claim 44 is allowable at least because of its dependence from claim 39 for the reasons discussed above.

Claim 44 further recites "wherein said first one pin and said neighboring pin are electrically coupled together to form a common electrical node." (Emphasis added). The applied combination of references further fails to teach or suggest this element of claim 44, for the reasons discussed above with claim 12. The Final Office Action asserts on page 7 thereof that *Soldavini* teaches this element in that it teaches a first one (27) and a second one (30) of its pins being electrically coupled together via internal circuitry to form a common electrical node. Appellant respectfully disagrees. While, the separate pins of *Soldavini's* circuit may be electrically coupled together via the internal circuitry, they are not coupled to form a common electrical node. Rather, the separate pins provide separate electrical nodes with disparate inputs/outputs present thereon at any given time. Integrated circuits commonly include separate pins that are electrically coupled by internal circuitry. For instance, a first pin may be for receiving power, another pin may be for ground, another pin may be for outputting a first output signal, while still another pin may be for outputting a different output signal. Such pins, as in the case of *Soldavini*, do not provide a common electrical node, but rather each provide a disparate node on which a different input/output signal may be present at any give time.

Cini, *Cyr*, and *Kwark* are not relied upon for resolving the above deficiencies of *Soldavini*, nor do they do so.

Thus, for this further reason, the rejection of claim 44 should be overturned.

B. Conclusion

In view of the above, Appellant requests that the board overturn the outstanding rejections of claims 1-19 and 21-44. Attached hereto are a Claims Appendix, Evidence Appendix, and Related Proceedings Appendix. As noted in the attached Evidence Appendix, no evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted. Also, as noted by the Related Proceedings Appendix, no related proceedings are referenced in II above, and thus no copies of decisions in related proceedings are provided.

The required $500.00 fee for this response is enclosed. If any additional fee is due, please charge Deposit Account No. 06-2380, under order No. 49581/P042US/10315832, from which the undersigned is authorized to draw.

Respectfully submitted,

By: _____
Jody C. Bishop
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VIII. Claims Appendix

Claims Involved in the Appeal of Application Serial No. 10/807,789:

1. An integrated circuit comprising:

internal circuitry;

package having at least two pins;

a first carrier communicatively coupling said internal circuitry with a first one of said at least two pins, wherein said first carrier carries a signal of a first polarity;

a second carrier communicatively coupling said internal circuitry with said first one of said at least two pins, wherein said second carrier carries a signal of a polarity opposite said first polarity;

a third carrier communicatively coupling said internal circuitry with a second one of said at least two pins, wherein said third carrier carries a signal of said first polarity; and

a fourth carrier communicatively coupling said internal circuitry with said second one of said at least two pins, wherein said fourth carrier carries a signal of a polarity opposite said first polarity.

2. The integrated circuit of claim 1 wherein said package encloses said circuitry therein.

3. The integrated circuit of claim 1 wherein said at least two pins provides an interface for said internal circuitry to a component external to said integrated circuit.

4. The integrated circuit of claim 1 wherein said first, second, third, and fourth carriers are bond wires.

5. The integrated circuit of claim 1 wherein said internal circuitry comprises resonant frequency circuitry.

6. The integrated circuit of claim 5 wherein said resonant frequency circuitry comprises a voltage controlled oscillator.

7. The integrated circuit of claim 6 wherein said voltage controlled oscillator is a differential voltage controlled oscillator.

8. The integrated circuit of claim 5 wherein said resonant frequency circuitry comprises at least one selected from the group consisting of: oscillator, resonant tank, filter, and matching circuit.

9. The integrated circuit of claim 1 wherein said resonant frequency circuitry comprises a resonant tank.

10. The integrated circuit of claim 9 wherein said resonant tank uses said first, second, third, and fourth carriers as inductors.

11. The integrated circuit of claim 1 wherein said internal circuitry uses said first, second, third, and fourth carriers as inductors.

12. The integrated circuit of claim 1 wherein said first one and said second one of said at least two pins are electrically coupled together to form a common electrical node.

13. The integrated circuit of claim 12 wherein said first one and said second one of said at least two pins are electrically coupled together external to said integrated circuit.

14. The integrated circuit of claim 12 wherein said first one and said second one of said at least two pins are electrically coupled together within said package of said integrated circuit.

15. The integrated circuit of claim 1 wherein said first, second, third, and fourth carriers are arranged in parallel interleaving the signal polarities carried thereby.

16. The integrated circuit of claim 1 wherein the carriers are arranged with said first carrier arranged as a neighbor to said second carrier, said second carrier arranged as a neighbor to said third carrier, and said third carrier arranged as a neighbor to said fourth carrier.

17. The integrated circuit of claim 1 wherein said first one and said second one of said pins are neighbor pins in said package.

18. A method comprising:

coupling a first carrier from an internal resonant frequency circuitry of an integrated circuit to an electrically common interface of the integrated circuit's package, wherein said first carrier is arranged to carry signals of a first polarity;

coupling a second carrier from said internal resonant frequency circuitry of said integrated circuit to said electrically common interface of the integrated circuit's package, wherein said second carrier is arranged to carry signals of a polarity opposite said first polarity; and

coupling a third carrier from said internal resonant frequency circuitry of said integrated circuit to said electrically common interface of the integrated circuit's package, wherein said third carrier is arranged to carry signals of said first polarity.

19. The method of claim 18 wherein said coupling said first carrier from said internal resonant frequency circuitry to said electrically common interface comprises bonding a first wire from said internal resonant frequency circuitry to said electrically common interface, wherein said coupling said second carrier from said internal resonant frequency circuitry to said electrically common interface comprises bonding a second wire from said internal resonant frequency circuitry to said electrically common interface, and wherein said coupling said third carrier from said internal resonant frequency circuitry to said electrically common interface comprises bonding a third wire from said internal resonant frequency circuitry to said electrically common interface.

20. (Cancelled)

21. The method of claim 18 wherein said electrically common interface comprises at least one pin.

22. The method of claim 21 wherein said electrically common interface comprises a plurality of pins that are electrically coupled together.

23. The method of claim 18 wherein said electrically common interface comprises a plurality of pins, further comprising:

electrically coupling said plurality of pins together external to said integrated circuit.

24. The method of claim 18 further comprising:

coupling a fourth carrier from said internal resonant frequency circuitry of said integrated circuit to said electrically common interface of the integrated circuit's package, wherein said fourth carrier is arranged to carry signals of a polarity opposite said first polarity.

25. The method of claim 24 wherein said electrically common interface comprises two pins that are electrically coupled together, said coupling said first, second, third, and fourth carriers from said internal resonant frequency circuitry to said electrically common interface comprises:

coupling said first and second carriers to a first one of said two pins; and

coupling said third and fourth carriers to second one of said two pins.

26. The method of claim 25 further comprising:

arranging said first, second, third, and fourth carriers to interleave the signal polarities carried thereby.

27. The method of claim 25 further comprising:

arranging said first, second, third, and fourth carriers such that the neighboring carriers of any given one of said first, second, third, and fourth carriers carry signals of opposite polarity relative to the polarity of signals carriers by said given one.

28. The method of claim 18 further comprising:

using said first, second, and third carriers as inductors for said internal resonant frequency circuitry.

29. The method of claim 18 further comprising:

arranging said first, second, and third carriers to interleave the signal polarities carried thereby.

30. The method of claim 18 wherein said internal resonant frequency circuitry comprises at least one selected from the group consisting of: oscillator, resonant tank, filter, and matching circuit.

31. The method of claim 18 wherein said internal resonant frequency circuitry comprises a resonant tank.

32. A system comprising:

resonant tank circuitry implemented in a package that provides a plurality of interface means that are electrically coupled together to form an electrically common interface;

first coupling means for communicatively coupling said resonant tank circuitry to one of said plurality of interface means, wherein said first coupling means carries a signal of a first polarity; and

second coupling means for communicatively coupling said resonant tank circuitry to one of said plurality of interface means, wherein said second coupling means carries a signal of polarity opposite said first polarity.

33. The system of claim 32 wherein said first coupling means and said second coupling means are used as inductors for said resonant tank circuitry.

34. The system of claim 32 further comprising:

third coupling means for communicatively coupling said resonant tank circuitry to one of said plurality of interface means, wherein said third coupling means carries a signal of said first polarity.

35. The system of claim 34 further comprising:

fourth coupling means for communicatively coupling said resonant tank circuitry to one of said plurality of interface means, wherein said fourth coupling means carries a signal of polarity opposite said first polarity.

36. The system of claim 35 wherein said first and second coupling means couple said resonant tank circuitry to a first one of said plurality of interface means, and wherein said third and fourth coupling means couple said resonant tank circuitry to a second one of said plurality of interface means.

37. The system of claim 32 wherein said plurality of interface means are electrically coupled together external to said package.

38. The system of claim 32 further comprising a board to which said package is electrically coupled, wherein said plurality of interface means are electrically coupled together on said board.

39. A system comprising:

internal circuitry implemented in a package that provides a plurality of pins;

a first plurality of carriers communicatively coupling said internal circuitry to a first one of said plurality of pins, wherein said first plurality of carriers are used as inductors for said internal circuitry, and wherein at least one of said first plurality of carriers carries a signal of a first polarity and at least one other of said first plurality of carriers carries a signal of polarity opposite said first polarity;

a second plurality of carriers communicatively coupling said internal circuitry to a neighboring pin of said first one of said plurality of pins, wherein said second plurality of carriers are used as inductors for said internal circuitry, and wherein at least one of said second plurality of carriers carries a signal of said first polarity and at least one other of said second plurality of carriers carries a signal of polarity opposite said first polarity; and

said first plurality of carriers and said second plurality of carriers arranged to interleave the polarities of signals carried thereby.

40. The system of claim 39 wherein said plurality of pins each provide an interface for communicatively coupling to a component external to the package.

41. The system of claim 40 wherein the external component electrically couples said first pin and said neighboring pin together.

42. The system of claim 39 wherein said internal circuitry comprises resonant tank circuitry.

43. The system of claim 42 wherein said resonant tank circuitry uses said first plurality of carriers and said second plurality of carriers as inductors.

44. The system of claim 39 wherein said first one pin and said neighboring pin are electrically coupled together to form a common electrical node.

IX. Evidence Appendix

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. Related Proceedings Appendix

No related proceedings are referenced in II above, and thus no copies of decisions in related proceedings are provided.